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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/003,412	12/06/2001	Jeong-Sic Jeon	249/275	5396

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EXAMINER	
HASSANZADEH, PARVIZ	
ART UNIT	PAPER NUMBER
1763	

DATE MAILED: 10/20/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/003,412	JEON ET AL.	
	Examiner	Art Unit	
	Parviz Hassanzadeh	1763	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 August 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) *3,4,6,7,19 and 20* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,5 and 8-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 December 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *4/2003* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Election/Restrictions

Applicant's election without traverse of Species 1 in Paper No. 8/25/03 is acknowledged, claims 1, 2, 5, 8-18 are readable on elected species 1.

Claims 3, 4, 6, 7, 19 and 20 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected species 2-4, there being no *allowable* generic or linking claim. Election was made **without** traverse in Paper No. 8/25/03. It is noted that claim 7 depends on non-elected claim 6; and claim 19, requiring a second chamber having a smaller cross-sectional area than a first chamber, is readable on Fig. 3 (species 2) and Fig. 5 (species 4).

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipated by Hitachi (JP 9-181049-A).

Hitachi teaches an apparatus (Fig. 17) for manufacturing a semiconductor device using plasma, the apparatus comprising:

a chamber 4 having plasma generation region 12 and a plasma processing region for performing a manufacturing process on the semiconductor device 1 under a plasma atmosphere;

plasma electrode 6 (*plasma generating means*) adjacent the plasma generating region, the electrode 6 coupled to a power source 8 for generating a plasma; and

an insulating ring members 3, 3b which inherently would act as a plasma concentrating device reducing the size of the plasma processing region near the wafer as shown in Fig. 17 (*a plasma concentrating means for reducing the size of the plasma processing region near the semiconductor device to be processed compared to the size of a plasma generating region*) (abstract).

Claims 1, 16-18 are rejected under 35 U.S.C. 102(b) as being anticipated by Lymberopoulos et al (US Patent No. 6,085,688).

Lymberopoulos et al teach an apparatus (Fig. 5) for manufacturing a semiconductor device using plasma, the apparatus comprising:

a chamber 120 having plasma generation region and a plasma processing region for performing a manufacturing process on the semiconductor device 19 under a plasma atmosphere;

induction coils 110 (*plasma generating means*) adjacent the plasma generating region, the antenna 110 is coupled to a power source 116 for generating a plasma; and

a magnetic field generator including inductors 150a, 150b (*a plasma concentrating means for reducing the size of the plasma processing region near the semiconductor device to be processed compared to the size of a plasma generating region*) (column 5, line 3 through column 6, line 20). The plasma density distribution can be adjusted using the magnetic field generator.

Regarding claims 16-18: the induction coils 110 being disposed outside of the chamber; and the apparatus further includes a power source 115 coupled to a lower substrate support electrode 132 (column 4, lines 12-59).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 1, 16-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over admitted prior art (Fig. 1A, pages 2-3) in view of Hitachi (JP 9-181049-A).

Admitted prior art (Fig. 1A) teaches an apparatus for manufacturing a semiconductor device using plasma, the apparatus comprising:

a chamber 12 having plasma generation region 24 and a plasma processing region defined between plasma region and a wafer 30 for performing a manufacturing process on the semiconductor device 30 under a plasma atmosphere;

induction coils 14 (*plasma generating means*) adjacent the plasma generating region, the antenna coils 14 coupled to a power source 16 for generating a plasma.

the admitted prior art fails to teach *a plasma concentrating means for reducing the size of the plasma processing region near the semiconductor device to be processed compared to the size of a plasma generating region.*

Hitachi teaches an apparatus for plasma processing a wafer 1, the apparatus including an insulating ring members 3, 3b as shown in Fig. 17 covering the surface peripheral portion 1d of the wafer 1 in non-contacting manner so that a micro clearance 14 is formed between a portion of the photoresist film on the peripheral surface of the wafer and the insulating ring member3, thus, the passage of plasma towards side face 1a of the wafer is blocked by the clearance (abstract).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to implement the insulating ring member as taught by Hitachi in the apparatus of the admitted prior art in order to block the passage of plasma towards side face of the substrate. The insulating ring member inherently would act as a plasma concentrating device reducing the size of the plasma processing region near the wafer as shown in Fig. 17.

Further regarding claim 16-18: the apparatus of admitted prior art includes induction coils 14 (*plasma generating means*) installed outside of the chamber and is coupled to a plasma power source 16; and a lower electrode 26 supporting the substrate and being coupled to a second power source 18.

Claims 1, 2, 5, 8-13, 15, 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over admitted prior art (Fig. 1A, pages 2-3) in view of Tanaka (US Patent No. 6,296,747 B1).

Admitted prior art (Fig. 1A) teaches an apparatus for manufacturing a semiconductor device using plasma, the apparatus comprising:

a chamber 12 having plasma generation region 24 and a plasma processing region defined between plasma region and a wafer 30 for performing a manufacturing process on the semiconductor device 30 under a plasma atmosphere;

induction coils 14 (*plasma generating means*) adjacent the plasma generating region, the antenna coils 14 coupled to a power source 16 for generating a plasma.

the admitted prior art fails to teach *a plasma concentrating means for reducing the size of the plasma processing region near the semiconductor device to be processed compared to the size of a plasma generating region.*

Tanaka teaches an apparatus (Fig. 3) for plasma processing a wafer 18, the apparatus including an inner shield 96 for protecting the chamber wall from being coated during plasma processing (column 1, lines 39-50 and column 5, lines 30-40).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to implement the shielding mechanism as taught by Takana in the apparatus of the admitted prior art in order to protect the chamber wall from being coated during processing. The shielding member particularly the inner shield 96 would inherently act as a plasma concentrating device reducing the size of the plasma processing region near the wafer as the inner shield 96 having a generally smaller cross section at the lower portion compared to the upper portion.

Regarding claim 2: the apparatus of admitted prior art further includes:

a lower electrode 26 supporting an electrostatic chuck 28 for supporting the wafer 30 ;

an insulating plate 20 having a second length similar to the first length of the lower electrode.

Admitted prior art fails to teach the lower electrode having a length smaller than the upper insulating plate.

Takana teach a substrate support electrode where the diameter support electrode is slightly larger than the diameter of the wafer as shown in Figs. 3 and 4.
Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to use wafer support electrode as taught by Takana in the apparatus of admitted prior art as an art recognized equivalent for the same purpose. See MPEP 2144.06, Art Recognized Equivalent for the Same Purpose, Substituting Equivalents Known for the Same Purpose (in re Fout, 675 F.2d 297, 213 USPQ 532 (CCPA 1982)).

Further, the inner shield 96 of Takana corresponds to the confinement layer contacting the insulating plate, forming an acute angle and extending toward an edge of the lower electrode.

Further regarding claim 5: the apparatus of admitted prior art includes a insulating plate 20 which is a circular plate having a predetermined diameter or length.

Further regarding claim 8: the apparatus of admitted prior art includes a chuck 28.

Further regarding claim 9-13, 15: It was held in re Gardner v. TEC Systems, Inc., 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984) that where the only difference between the prior art and the claims was a recitation of relative dimensions of the claimed device and a device having the claimed relative dimensions would not perform differently than the prior art device, the claimed device was not patentably distinct from the prior art device.

Further regarding claims 16-18: the apparatus of admitted prior art includes induction coils 14 (*plasma generating means*) installed outside of the chamber and is coupled to a plasma power source 16; and a lower electrode 26 supporting the substrate and being coupled to a second power source 18.

Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over admitted prior art (Fig. 1A, pages 2-3) in view of Tanaka (US Patent No. 6,296,747 B1) as applied to claims 1, 2, 5, 8-13, 15,18 above, and further in view of Conte et al (US Patent No. 6,299,746 B1).

Admitted prior art (Fig. 1A) in view of Tanaka teach all limitations of the claims as discussed above except for the shield member having an acute angle between 45 and 89 degree.

Conte et al teach a vapor deposition apparatus (Fig. 1) including screens 20, 20' for confining the process region 21 from the rest of the chamber 11, wherein the screens 20, 20 having a generally cylindrical shape reducing in diameter as it approaches the substrate support as shown in Fig. 1 (column 4, lines 22-65).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the shape of the screen as taught by Conte in the shield member of Takana in order to further confine the plasma processing volume toward the substrate and away from the chamber wall.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Parviz Hassanzadeh whose telephone number is (703)308-2050. The examiner can normally be reached on Tuesday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Gregory Mills can be reached on (703)308-1633. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)308-0661.

P. Hassanzadeh

Parviz Hassanzadeh
Primary Examiner
Art Unit 1763

September 20, 2003